

IP Datasheet 20GSa/s 12-Bit RF-ADC IP

20GSa/s 12-Bit Analogue-to-Digital Converter (ADC)

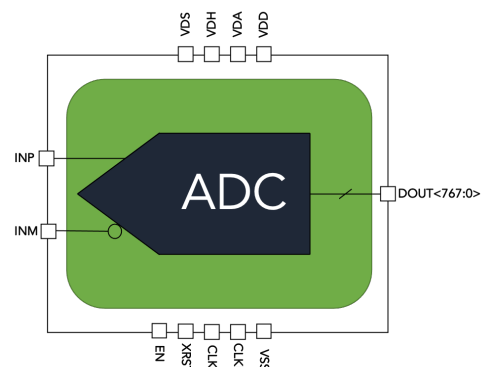
Description

1-VIA's high-speed low-power RF-ADC is targeted at upcoming telecommunication markets such as 5G and Satellite Communications. The RF-ADC has an effective 3dB bandwidth > 9GHz and 10 Effective Number of Bits (ENOB), making it an ideal candidate for FR1 (sub-6 GHz) and FR2 (mmWave 6-100 GHz) 5G deployment scenarios.

The ADC is a standalone macro which employs calibration of time interleaving skew, linearity and offset both at start-up and continuously in the background.

Key Features

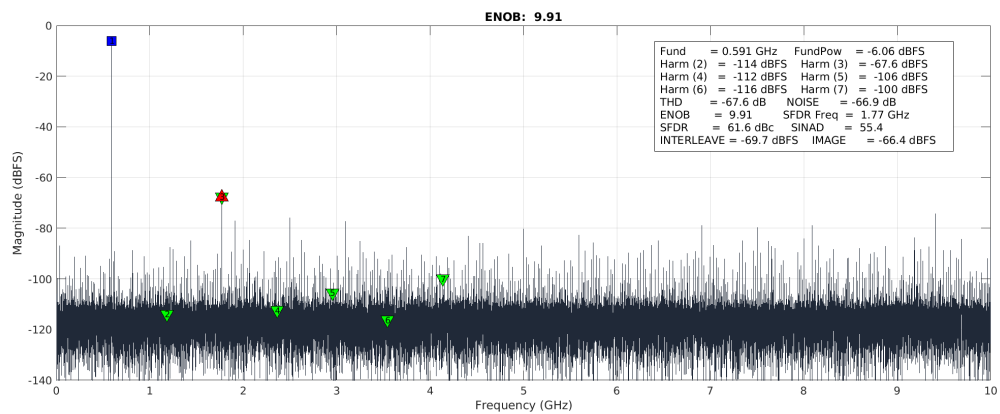
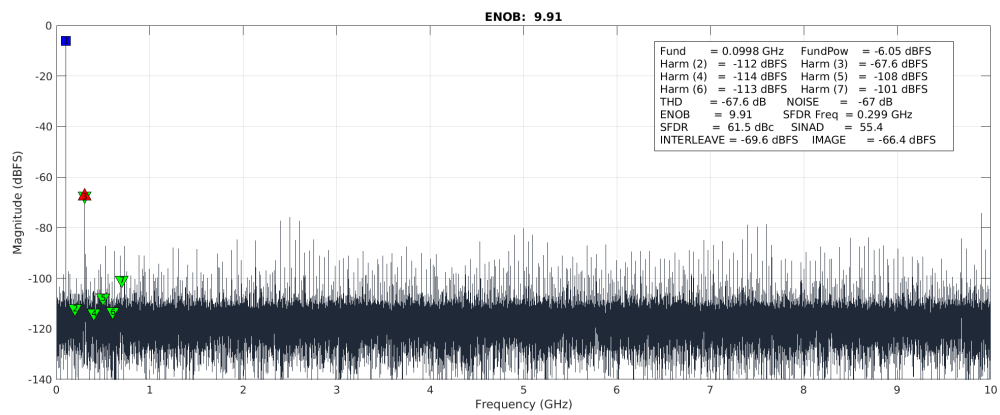
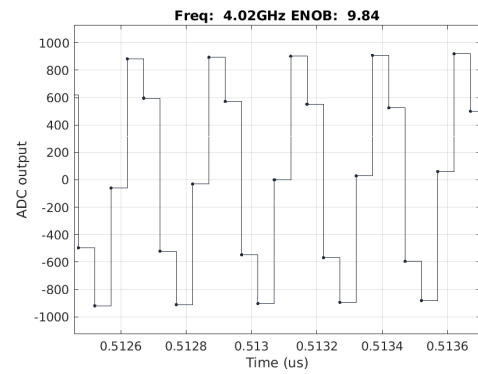
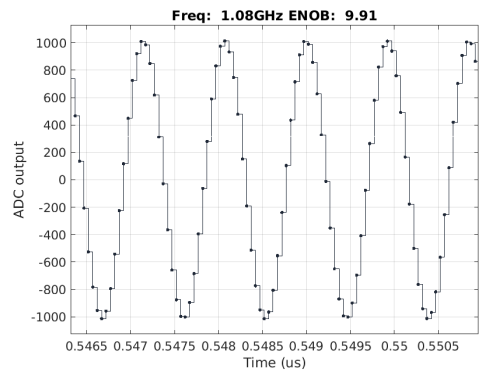
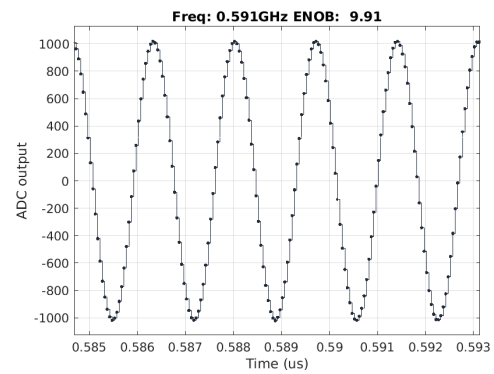
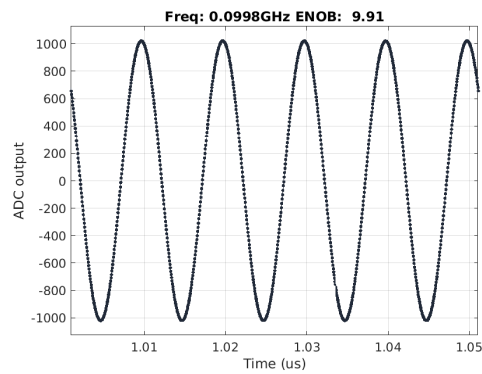
- TSMC: 12/16nm CMOS FinFET
- Resolution: 12-bit
- Sampling rate: 20GSa/s
- Power supplies: 1.8V, 1.2V, 1V and 0.8V
- Power consumption: 800mW
- Differential analog input: $1V_{ppd}$
- 3dB Input bandwidth: > 9GHz
- DNL: ± 0.5 LSB
- INL: ± 0.5 LSB
- SNDR: 61.5dBc
- Background time interleaving skew, linearity and offset calibration

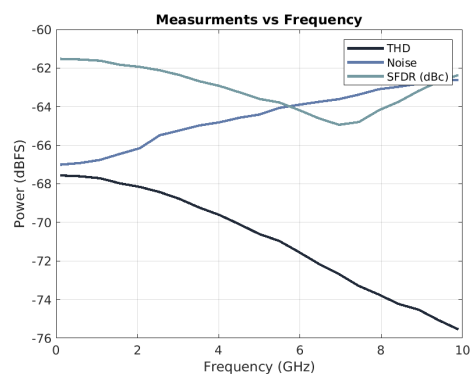
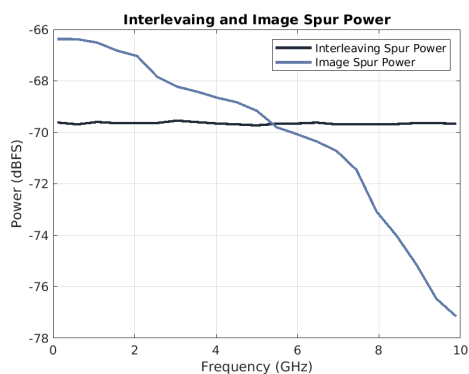
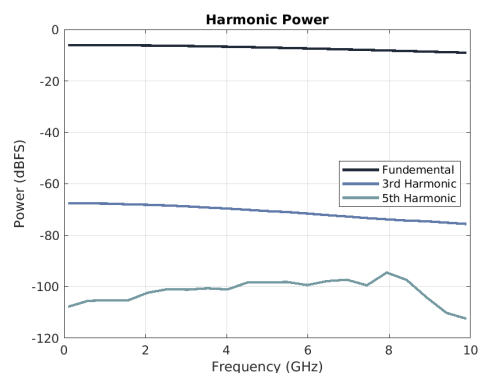
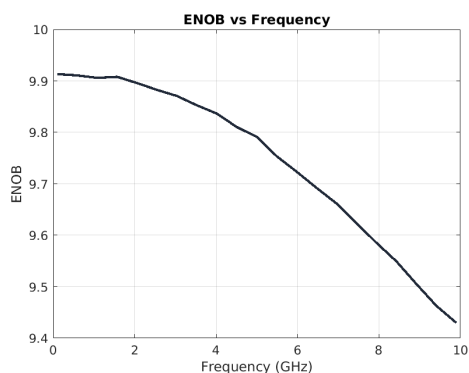
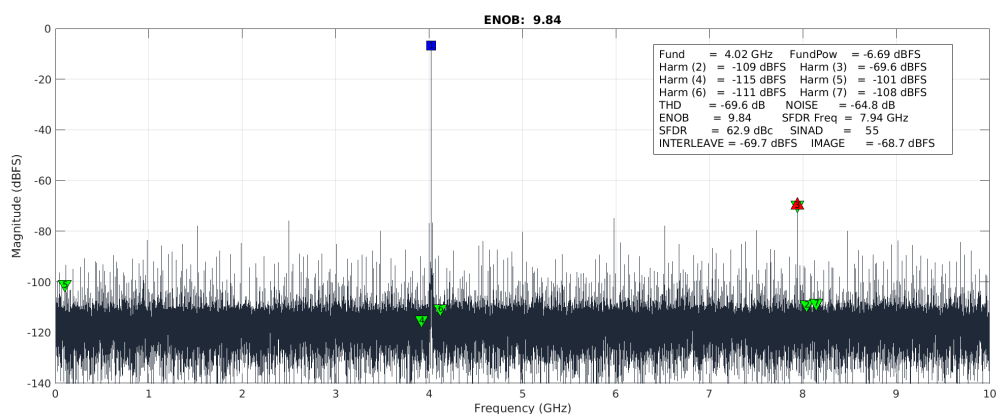
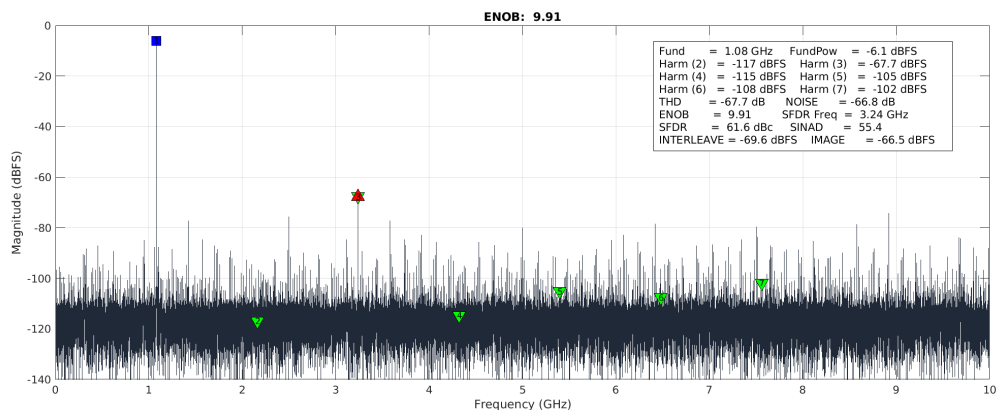


Applications

- 5G Base stations
- Automotive Driver Assistance Systems (ADAS)
- Direct-RF
- Multi-carrier and Multi-standard wireless infrastructure
- Satellite communications
- Test equipment

Performance Results





IP Deliverables

- Datasheet
- Characterization report
- Layout view (GDSII)
- Abstract view (LEF)
- Timing View (LIB)
- Behavioural model (Verilog)
- Integration guidelines and support


Above deliverables are subject to agreement.

Disclaimer

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About 1-VIA

At 1-VIA we are continuously developing state-of-the-art, high-speed and low-power transceivers targeting next-generation satellite, data centre, telecommunications and automotive markets. With some of the industry's most skilled and experienced analog/mixed-signal IC designers onboard we have a combined experience of more than 100 years in cutting-edge silicon design of high-speed ADC, DAC and SerDes.

	UK Office	Bulgaria Office
	Siena Court	1 Yambolen Street
	The Broadway	Yambol
	Maidenhead	8600
	SL6 1NJ	
	Contact: sales@1-via.com	
	Website: https://www.1-via.com	